ACPM-7355

UMTS Dual-Band 4x5mm Power Amplifier Module (Band2/Band5)

Data Sheet

Description

The ACPM-7355 is a dual-band PAM (Power Amplifier Module) designed for UMTS Band2 and Band5. The ACPM-7355 meets stringent UMTS linearity requirements. The 4mmx5mm form factor 14-pin surface mount package is self contained, incorporating 50ohm input and output matching networks

The ACPM-7355 features 5th generation of CoolPAM circuit technology which supports 3 modes – bypass, mid and high power modes. The CoolPAM is stage bypass technology which enables power amplifier to lower power consumption. Active bypass feature is added to 5th generation to enhance power added efficiency at low output range and this technology extends talk time of mobiles more by further saving power amplifier's current consumption.

The power amplifier is manufactured on an advanced InGaP HBT (hetero-junction Bipolar Transistor) MMIC (microwave monolithic integrated circuit) technology offering state-of-the-art reliability, temperature stability and ruggedness.

The Module is housed in a cost effective, small and thin 4x5mm package.

Features

- Dual-Band PA (Band2 and Band5)
- Small Size (4x5mm)
- Thin Package (1.0mm typ)
- Excellent Linearity
- 3-mode power control
- Bypass / Mid Power Mode / High Power Mode
  High Efficiency at max output power
- 14-pin surface mounting package
- Internal 50ohm matching networks for both RF input and output
- Lead-free, RoHS compliant, Green

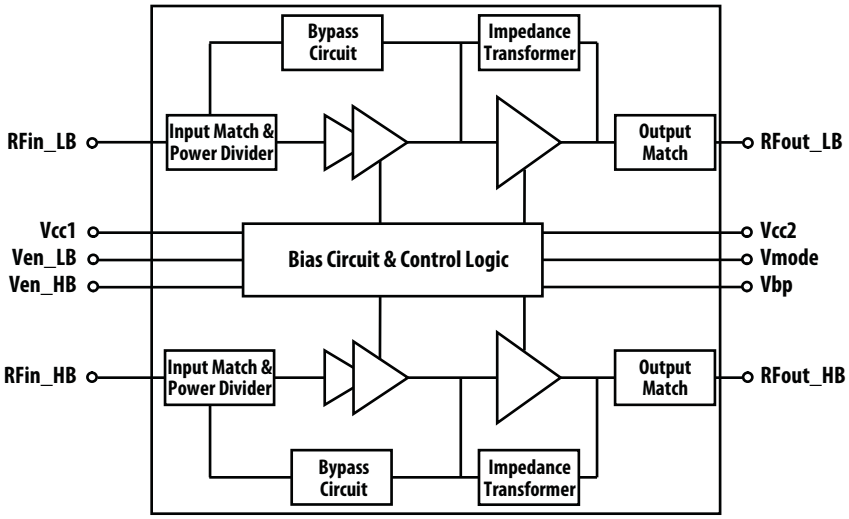
Applications

- UMTS Band2 and Band5

Ordering Information

Part Number	Number of Devices	Container
ACPM-7355-TR1	1000	178mm (7") Tape/Reel
ACPM-7355-BLK	100	Bulk

Block Diagram



Absolute Maximum Ratings

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below typical value.

Operation of any single parameter outside these conditions with the remaining parameters set at or below typical values may result in permanent damage.

Description	Min	Typ	Max	Unit	Associated Pins
RF Input Power (high power mode) Output power (bypass mode) Output power (mid power mode)		0	10 10 18	dBm	RFIn_Hi, RFIn_Low RFOut_Hi, RFOut_Low RFOut_Hi, RFOut_Low
DC Supply Voltage	0	3.4	5.0	V	Vcc1, Vcc2
Enable Voltage	0	2.6	3.3	V	Ven_Low, Ven_Hi
Mode Control Voltage	0	2.6	3.3	V	Vmode
Bypass Control	0	2.6	3.3	V	Vbp
Storage Temperature	-55	25	+125	°C	

Recommended Operating Condition

Description		Min	Typ	Max	Unit
DC Supply Voltage		3.2	3.4	4.2	V
Enable Voltage (Ven_Low, Ven_Hi)	 LOW HIGH	 0 1.35	 0 2.6	 0.5 3.1	 V V
Mode Control Voltage (Vmode)	 LOW HIGH	 0 1.35	 0 2.6	 0.5 3.1	 V V
Bypass Control Voltage (Vbp)	 LOW HIGH	 0 1.35	 0 2.6	 0.5 3.1	 V V
Operating Frequency Band5 Band2		 824 1850		 849 1910	 MHz MHz
Ambient Temperature		-30	25	85	°C

Operating Logic Table

Power Mode	Ven_Low, Ven_Hi	Vbp	Vmode	Pout (Rel99)	Pout (HSDPA, HSUPA MPR=0dB)
High Power Mode	HIGH	LOW	LOW	~27.0dBm (Band5) ~27.5dBm(Band2)	~26.0dBm (Band5) ~ 26.5dBm (Band2)
Mid Power Mode	HIGH	LOW	HIGH	~17dBm	~16dBm
Bypass Mode	HIGH	HIGH	HIGH	~8dBm	~7dBm
Shut Down Mode	LOW	LOW	LOW	–	–

Electrical Characteristics in Band5

– Conditions: Vcc = 3.4V, Ven_Low = 2.6V, T = 25°C, Zin/Zout = 50ohm

– Signal Configuration: 3GPP (DPCCH+1DPDCH) Up-Link unless specified otherwise

Characteristics		Condition	Min	Typ	Max	Unit
Operating Frequency Range			824	–	849	MHz
Gain		High Power Mode, Pout=27dBm	24	28.5		dB
		Mid Power Mode, Pout=17dBm	15	19.5		dB
		Bypass Power Mode, Pout=8dBm	10	15		dB
Total Supply Current		High Power Mode, Pout=27dBm		380	440	mA
		Mid Power Mode, Pout=17dBm		70	100	mA
		Bypass Power Mode, Pout=8dBm		13.5	20	mA
Quiescent Current		High Power Mode	70	95	120	mA
		Mid Power Mode	10	20	30	mA
		Bypass Mode	2	3.4	5	mA
Enable Current		High Power Mode		10		μA
		Mid Power Mode		10		μA
		Bypass Mode		10		μA
Mode Control Current		Mid Power Mode		5		μA
		Bypass Mode		5		μA
Bypass Control Current					100	μA
Total Current in Power-down mode		Ven_Low=0V, Vmode=0V, Vbp=0V		0.2	5	μA
Adjacent Channel Leakage Ratio	5 MHz offset 10 MHz offset	High Power Mode, Pout=27dBm		-42 -55	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	High Power Mode, Pout=26dBm (HSDPA, HSUPA MPR=0dB)		-40 -51	-35 -46	dBc dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout=17dBm		-49 -61	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout=16dBm (HSDPA, HSUPA MPR=0dB)		-47 -59	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Bypass Mode, Pout=8dBm		-41 -58	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Bypass Mode, Pout=7dBm (HSDPA, HSUPA MPR=0dB)		-40 -58	-36 -46	dBc dBc
Harmonic Suppression	Second Third	High Power Mode, Pout=27dBm		-37 -72	-30 -40	dBc dBc
Input VSWR				2:1	2.5:1	
Stability (Spurious Output)		In-Band Load VSWR <= 5:1, All Phase Out of Band Load VSWR <= 10:1, All Phase Forwarded power fixed			-60	dBc
Rx Band Noise Power				-135.5	-133	dBm/Hz
GPS Band Noise				-156	-140	dBm/Hz
Phase Discontinuity		mid power mode ↔ high power mode, at Pout=17dBm low power mode ↔ mid power mode, at Pout=8dBm		36		deg deg
Ruggedness		No Damage Pout<27dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

Electrical Characteristics in Band2

– Conditions: Vcc = 3.4V, Ven_Hi = 2.6V, T = 25°C, Zin/Zout = 50ohm

– Signal Configuration: 3GPP (DPCCH+1DPDCH) Up-Link unless specified otherwise

Characteristics		Condition	Min.	Typ.	Max.	Unit
Operating Frequency Range			1850	–	1910	MHz
Gain		High Power Mode, Pout=27.5dBm	24	28		dB
		Mid Power Mode, Pout=17dBm	15	21.5		dB
		Bypass Power Mode, Pout=8dBm	9	13.5		dB
Total Supply Current		High Power Mode, Pout=27.5dBm		440	500	mA
		Mid Power Mode, Pout=17dBm		75	105	mA
		Bypass Power Mode, Pout=8dBm		12.5	20	mA
Quiescent Current		High Power Mode	75	100	125	mA
		Mid Power Mode	15	25	35	mA
		Bypass Mode	1.5	3	4.5	mA
Enable Current		High Power Mode		10		μA
		Mid Power Mode		10		μA
		Bypass Mode		10		μA
Mode Control Current		Mid Power Mode		5		μA
		Bypass Mode		5		μA
Bypass Control Current					100	μA
Total Current in Power-down mode		Ven_Hi=0V, Vmode=0V, Vbp=0V		0.2	5	μA
Adjacent Channel Leakage Ratio	5 MHz offset 10 MHz offset	High Power Mode, Pout=27.5dBm		-41 -51	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	High Power Mode, Pout=26.5dBm (HSDPA, HSUPA MPR=0dB)		-39 -52	-35 -46	dBc dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout=17dBm		-50 -64	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Mid Power Mode, Pout=16dBm (HSDPA, HSUPA MPR=0dB)		-49 -62	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Bypass Mode, Pout=8dBm		-43 -54	-36 -46	dBc dBc
	5 MHz offset 10 MHz offset	Bypass Mode, Pout=7dBm (HSDPA, HSUPA MPR=0dB)		-41 -55	-36 -46	dBc dBc
Harmonic Suppression	Second Third	High Power Mode, Pout=27.5 dBm		-52 -74	-30 -40	dBc dBc
Input VSWR				2:1	2.5:1	
Stability (Spurious Output)		In-Band Load VSWR <= 5:1, All Phase Out of Band Load VSWR <= 10:1, All Phase Forwarded power fixed			-60	dBc
Rx Band Noise Power				-138	-133	dBm/Hz
GPS Band Noise				-140	-136	dBm/Hz
Phase Discontinuity		mid power mode ↔ high power mode, at Pout=17dBm low power mode ↔ mid power mode, at Pout=8dBm		16 21		deg deg
Ruggedness		No Damage Pout<27.5dBm, Pin<10dBm, All phase High Power Mode			10:1	VSWR

HSDPA Signal configuration used:

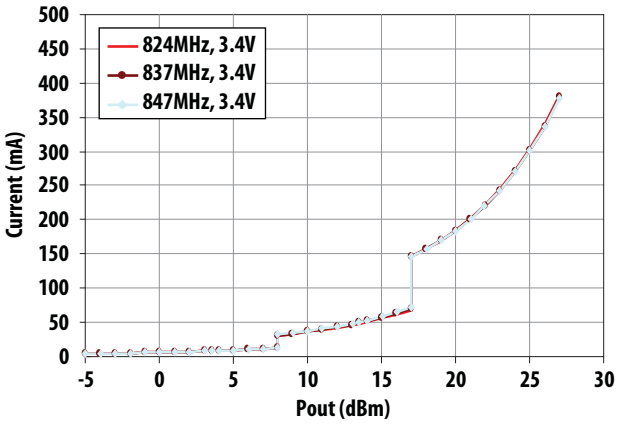
3GPP TS 34.121-1
Annex C (normative e): Measurement channels
C.10.1 UL reference measurement channel for HSDPA tests
Table C.10.1.4: β values for transmitter characteristics tests with HS-DPCCH
Sub-test 2 (CM=1.0, MPR=0.0)

HSUPA signal configuration used:

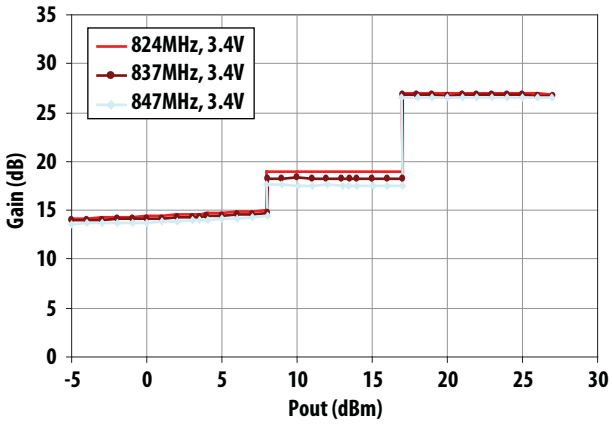
3GPP TS 34.121-1
Annex C (normative): Measurement channels
C.11.1 UL reference measurement channel for E-DCH tests
Table C.11.1.3: β values for transmitter characteristics tests with HS-DPCCH and E-DCH
Sub-test 1 (CM=1.0, MPR=0.0)

Characteristics Data of Band5

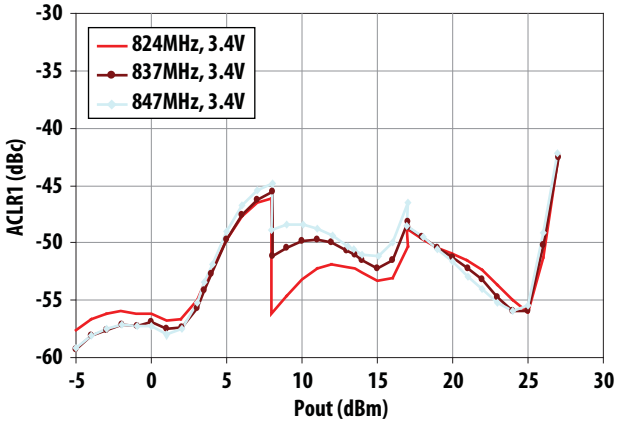
(Vcc = 3.4V, Ven_Low = 2.6, Vbp, Vmode = 0V or 2.6V, T = 25°C, Zin/Zout = 50ohm, Rel99)



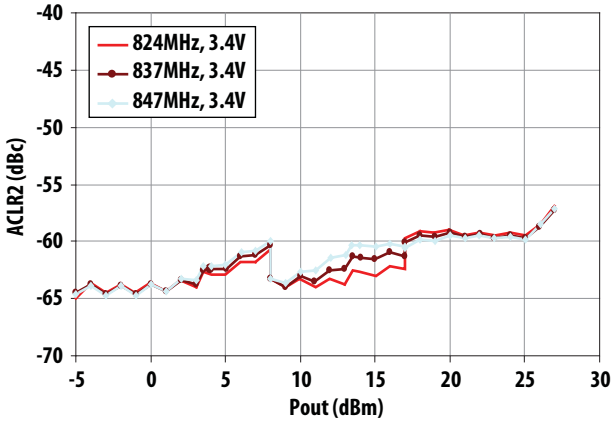
Total Current vs. Output Power



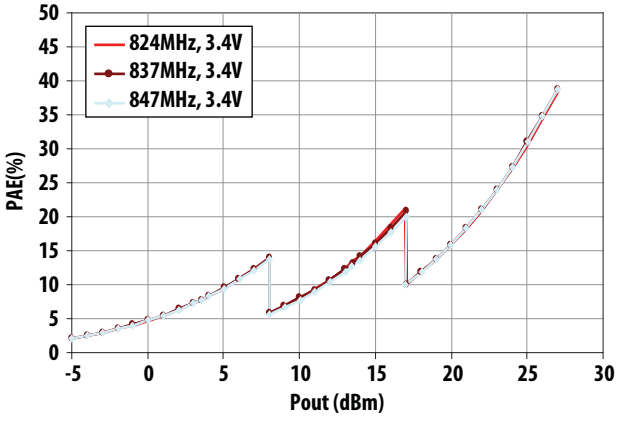
Gain vs. Output Power



Adjacent Channel Power Ratio 1 vs. Output Power



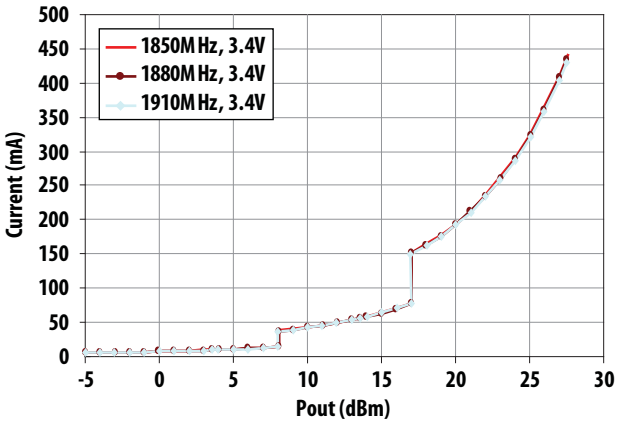
Adjacent Channel Power Ratio 2 vs. Output Power



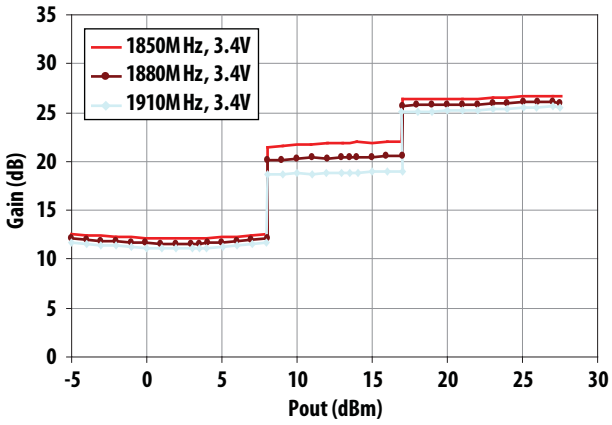
Power Added Efficiency vs. Output Power

Characteristics Data of Band2

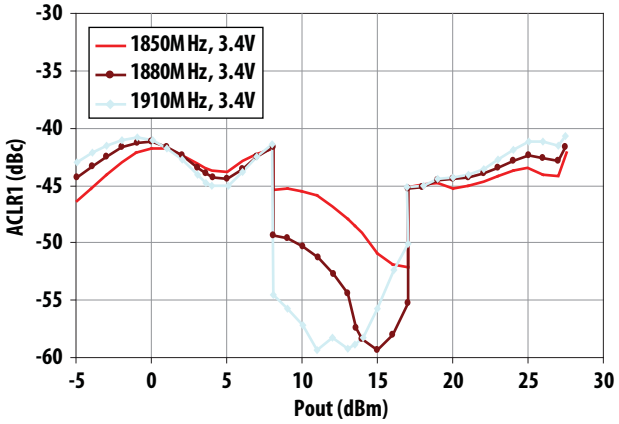
(Vcc = 3.4V, Ven_Hi = 2.6, Vbp and Vmode = 0V or 2.6V, T = 25°C, Zin/Zout = 50ohm, Rel99)



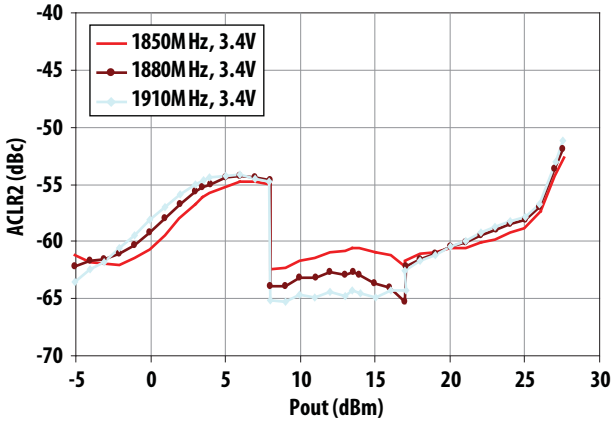
Total Current vs. Output Power



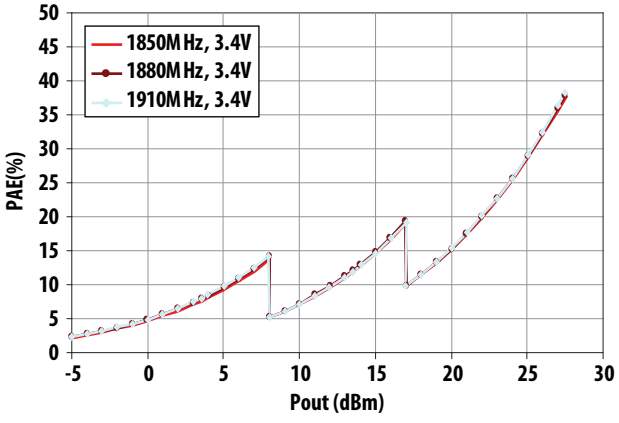
Gain vs. Output Power



Adjacent Channel Power Ratio 1 vs. Output Power



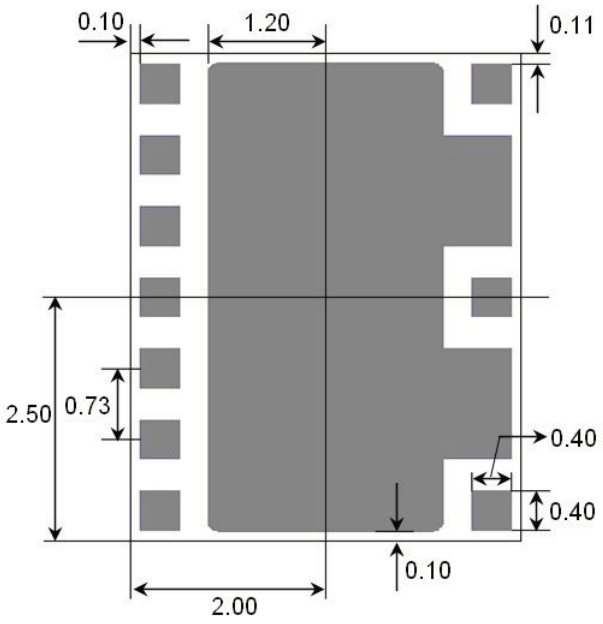
Adjacent Channel Power Ratio 2 vs. Output Power



Power Added Efficiency vs. Output Power

Footprint

All dimensions are in millimeters



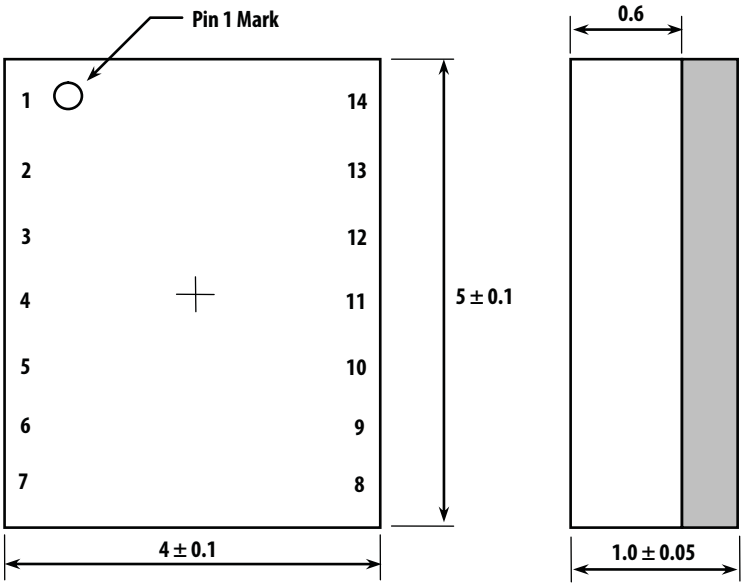
X-RAY TOP VIEW

PIN DESCRIPTIONS

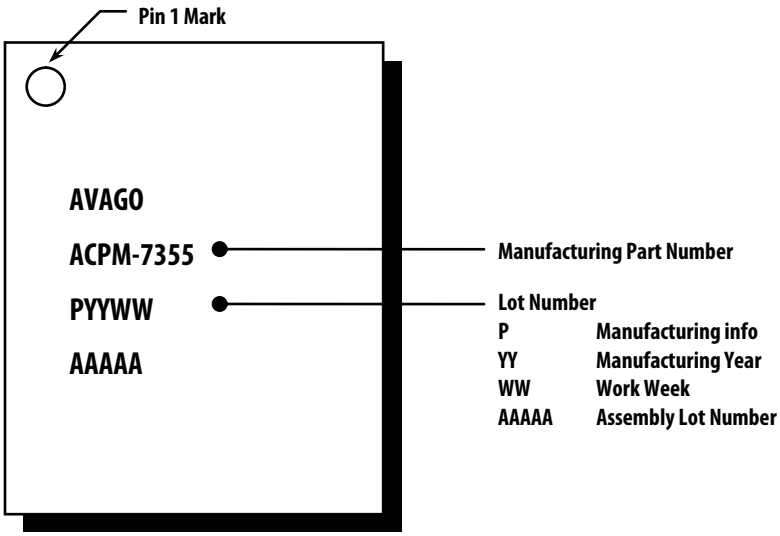
Pin #	Name	Description
1	RFIn_Low	Band5 RF Input
2	Vmode	Mode Control
3	Vbp	Bypass Control
4	Vcc1	Supply Voltage
5	Ven_Low	Band5 PA Enable
6	Ven_Hi	Band2 PA Enable
7	RFIn_Hi	Band2 RF Input
8	RFOut_Hi	Band2 RF Output
9	GND	Ground
10	GND	Ground
11	Vcc2	Supply Voltage
12	GND	Ground
13	GND	Ground
14	RFOut_Low	Band5 RF Output

Package Dimensions

All dimensions are in millimeters



Marking Specification



CoolPAM

Avago Technologies' CoolPAM is stage-bypass PA technology which saves more power compared with conventional PA. With this technology, the ACPM-7355 has very low quiescent current, and efficiencies at low and medium output power ranges are high.

Incorporation of bias circuit

The ACPM-7355 has internal bias circuit, which removes the need for external constant voltage source (LDO). PA on/off is controlled by Ven. This is digitally control pin.

3-mode power control with two mode control pins

The ACPM-7355 supports three power modes (bypass power mode/mid power mode/high power mode) with two mode control pins (Vmode and Vbp). This control scheme enables the ACPM-7355 to save power consumption more, which accordingly gives extended talk time.

PDF (probability density function) in the figure 1 showing distribution of output power of mobile in real field gives motivation for stage-bypass PA. Output power is less than 16dBm for most of operating time (during talking), so it is important to save power consumption at low and medium output power ranges.

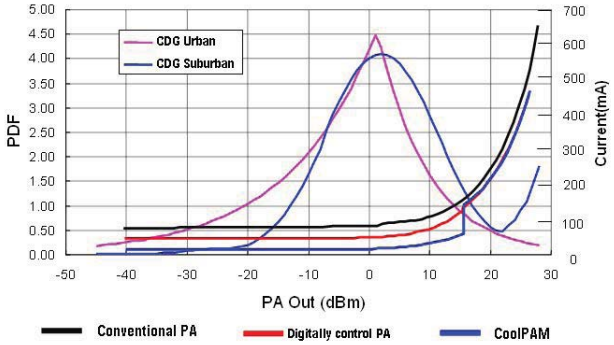


Figure 1 . PDF and Current

Average current & Talk time

Average current consumed by PA can be calculated by summing up current at each output power weighted with probability. So it is expressed with integration of multiplication of current and probability at each output power.

$$\text{Average current} = \int (\text{PDF} \times \text{Current}) dp$$

Talk time is extended more as average current consumption is lowered.

Mode control pins

Vmode and Vbp are digitally controlled by baseband and they control the operating mode of the PA. The logic table is summarized in the below table. These pins do not require constant voltage for interface.

Power Mode	Ven_Low, Ven_Hi	Vbp	Vmode	Pout (Rel99)	Pout (HSDPA, HSUPA MPR=0dB)
High Power Mode	HIGH	LOW	LOW	~27.0dBm (Band5) ~27.5dBm(Band2)	~26.0dBm (Band5) ~ 26.5dBm (Band2)
Mid Power Mode	HIGH	LOW	HIGH	~17dBm	~16dBm
Bypass Mode	HIGH	HIGH	HIGH	~8dBm	~7dBm
Shut Down Mode	LOW	LOW	LOW	–	–

Operating logic table.

UMTS PA performance comparison

– CoolPAM 4 and CoolPAM 5

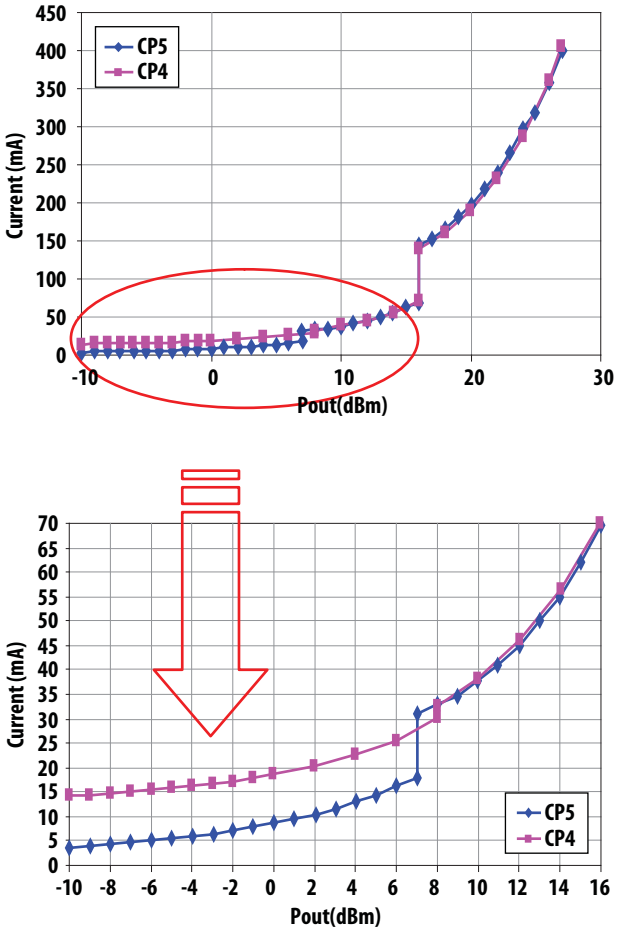


Figure 2. Icc Comparison of CP5 to CP4 (Avago CoolPAM)

The 5th generation of CoolPAM technology, ACPM-7355 can dramatically reduce Icc down to 3mA at bypass mode, which improves overall talk time and battery usage time of handset more compared with the CP4.

Application on mobile phone board

The figure 3 shows an application example in mobile. C5 and C6 should be placed close to pin4 and pin11. Bypass cap C1, C2, C3 and C4 should be also placed nearby from pin2, pin3, pin5 and pin6, respectively. The length of post-PA transmission line should be minimized to reduce line loss.

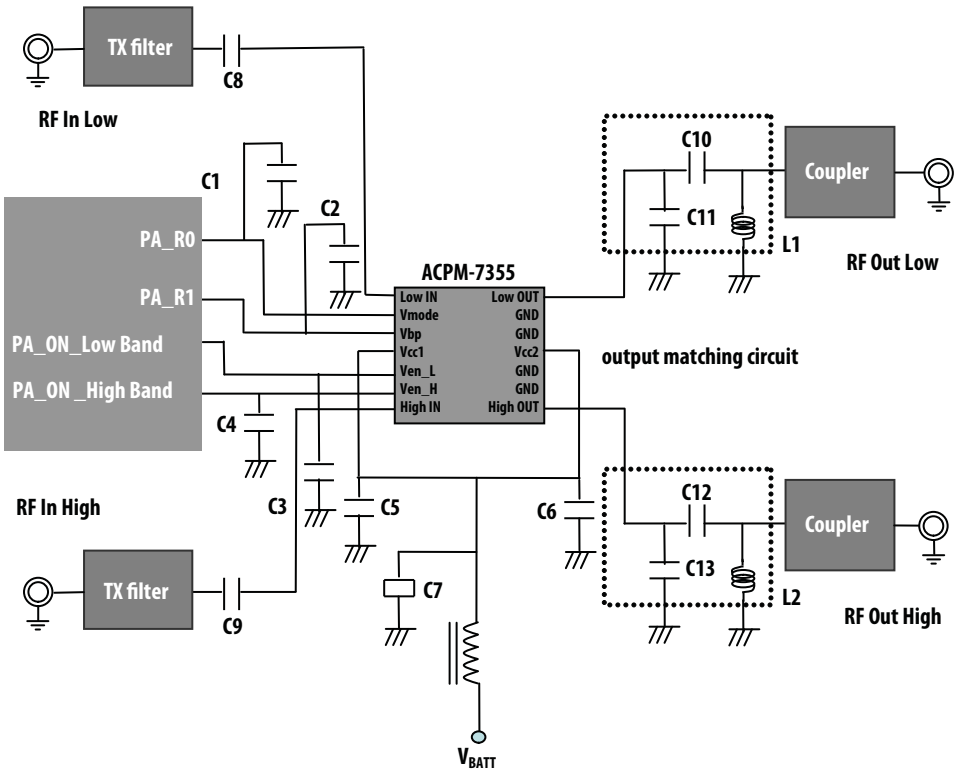


Figure 3. Peripheral Circuits

PCB layout and part placement on phone board

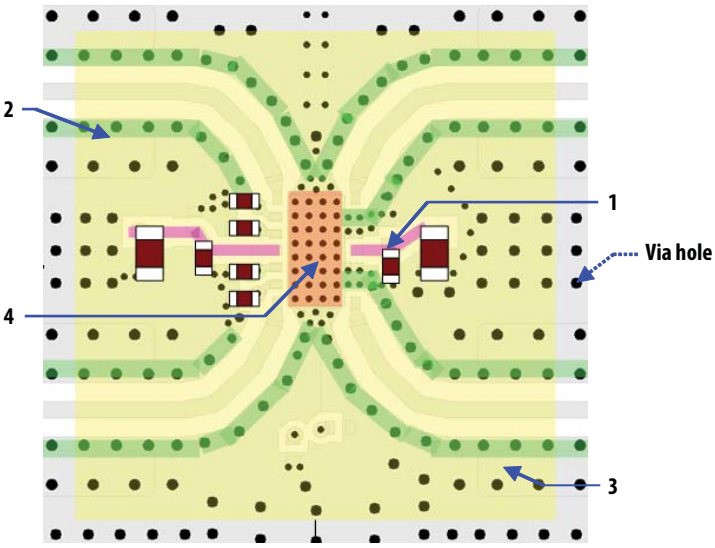
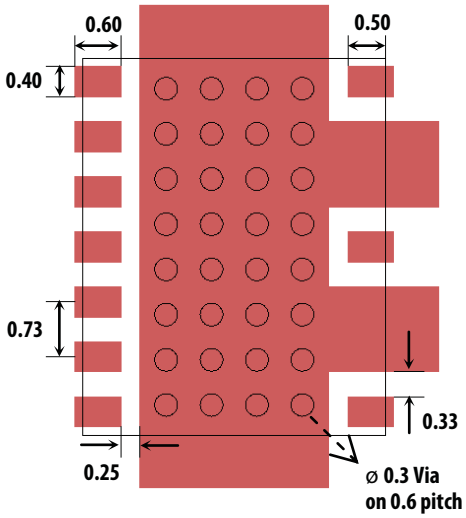


Figure 4. PCB guideline on phone board

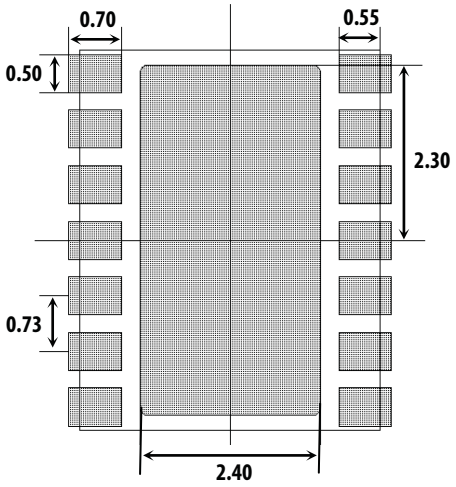
Notes:

1. To prevent voltage drop, make the bias lines as wide as possible (Pink line).
2. Use many via holes to fence off PA RF input and output traces for better isolation. Output signal of the PA should be isolated from input signal and the receive signal. Output signal should not be fed into PA input. (Green line)
3. Use via holes to connect outer ground plates to internal ground planes. They help heat spread out more easily and accordingly the board temperature can be lowered. They also help to improve RF stability (Yellow square).
4. PA which has a ground slug requires many via holes which go through all the layers (Red square).

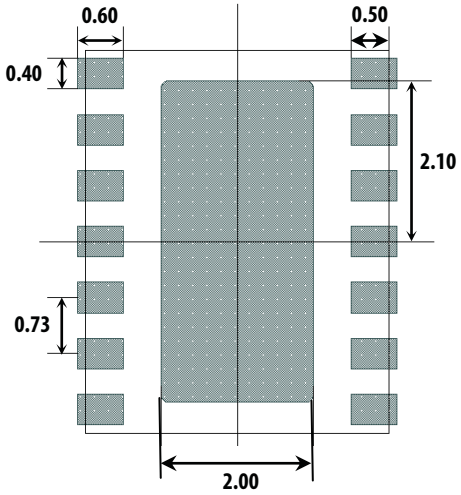
Metallization



Solder Mask Opening



Solder Paste Stencil Aperture



PCB Design Guidelines

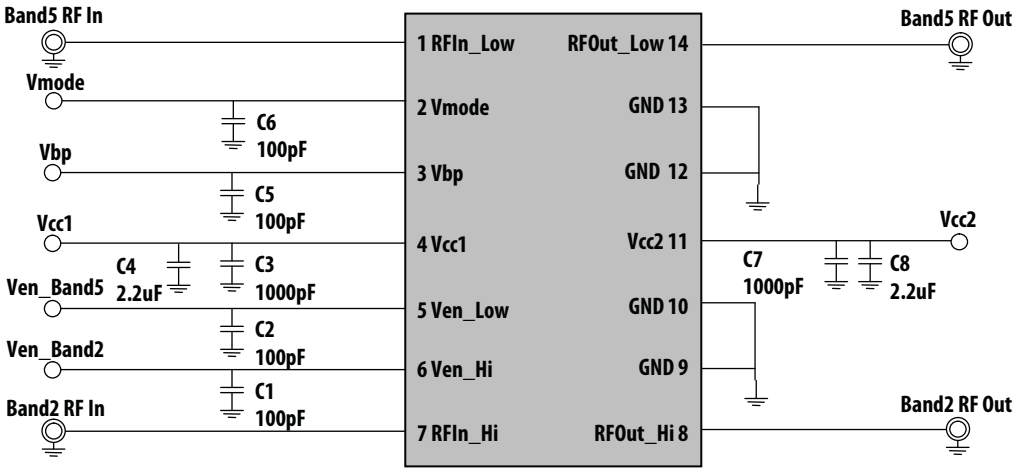
The recommended PCB land pattern is shown in figures on the left side. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

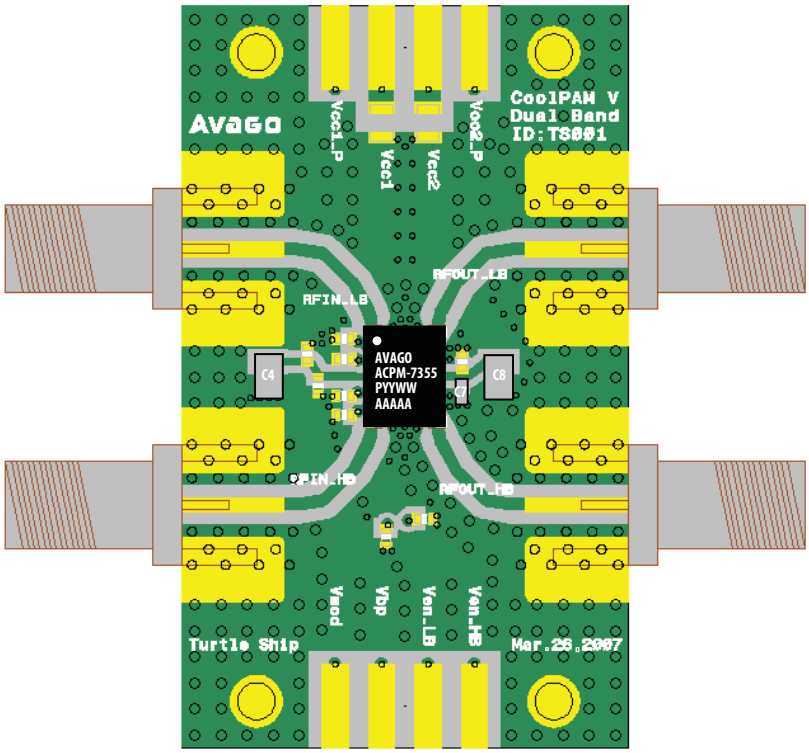
A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown here. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm(4mils) or 0.127mm(5mils) thick stainless steel which is capable of producing the required fine stencil outline.

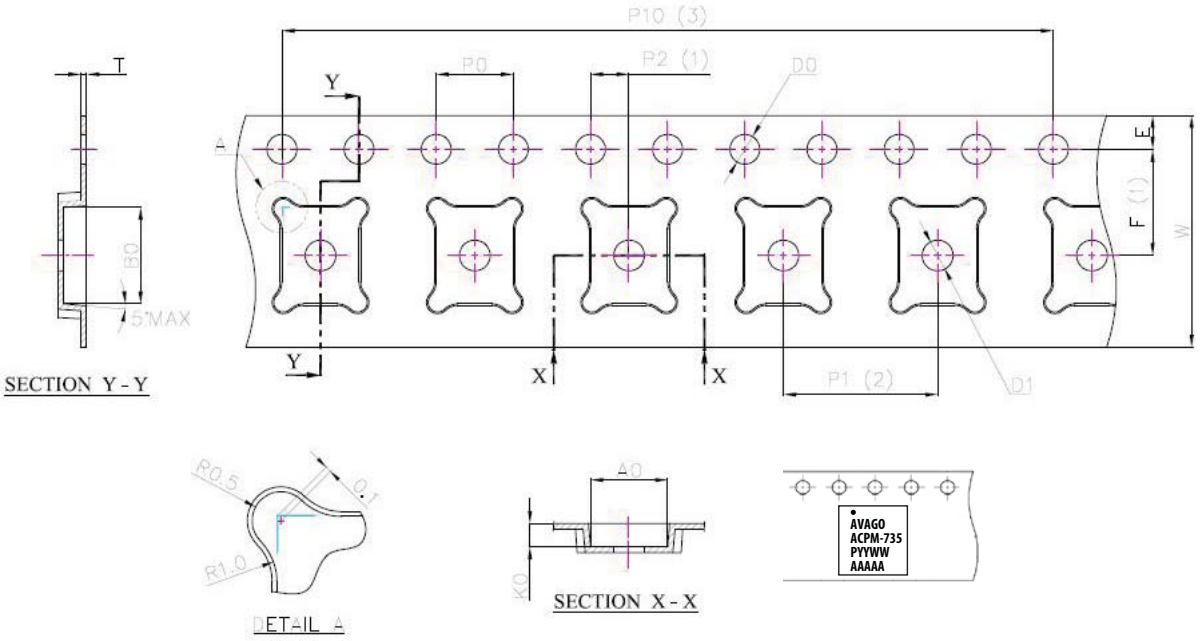
Evaluation Board Schematic



Evaluation Board Description



Tape and Reel Information



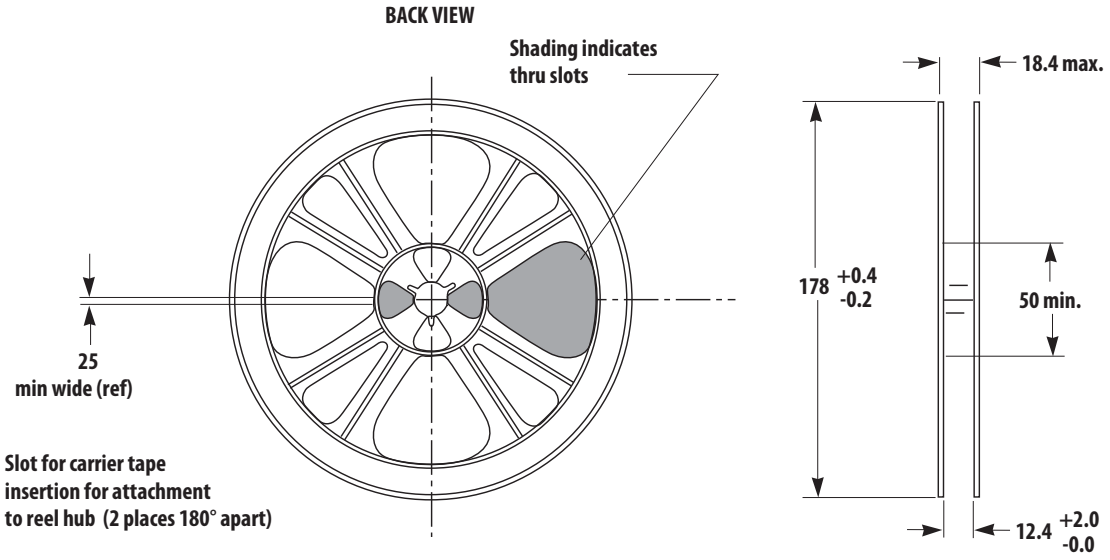
Dimension List

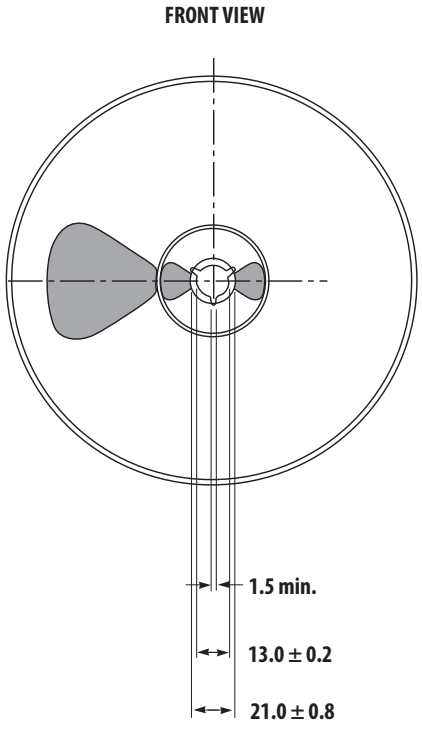
Dimension	Millimeter
A0	4.40±0.10
B0	4.40±0.10
K0	1.70±0.10
D0	1.55±0.05
D1	1.60±0.10
P0	4.00±0.10
P1	8.00±0.10

Dimension	Millimeter
P2	2.00±0.05
P10	40.00±0.20
E	1.75±0.10
F	5.50±0.05
W	12.00±0.30
T	0.30±0.05

Tape and Reel Format – 4 mm x 5 mm

Reel Drawing





NOTES:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance (c of c) shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm)

Plastic Reel Format (all dimensions are in millimeters)

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

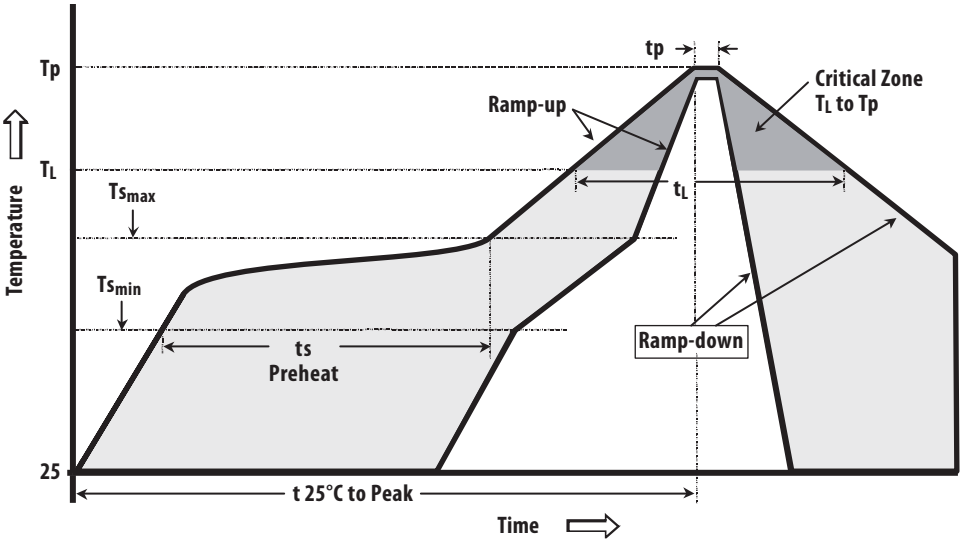
ACPM-7355 is MSL3. Thus, according to the J-STD-033 p.10, the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the ACPM-7355 is targeted at 260°C +0/-5°C. Figure and table on next page show typical SMT profile for maximum temperature of 260 +0/-5°C.

Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient =< 30°C/60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note :
1. The MSL Level is marked on the MSL Label on each shipping bag.

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 +0/-5°C

Typical SMT Reflow Profile for Maximum Temperature = 260 +0/ -5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C/sec max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 100°C 150°C 60-120 sec	 150°C 200°C 60-120 sec
Tsmax to TL – Ramp-up Rate		 3°C/sec max
Time maintained above: – Temperature (TL) – Time (TL)	 183°C 60-150 sec	 217°C 60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.6.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours with factory conditions <30°C and 60% RH as listed in the Table 5-1 on the J-STD-020D p.6.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above has not been satisfied. The baking conditions are listed in the Table 4-1 on the J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework
Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 andIPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in table of Moisture Classification Level and Floor Life. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table on follwoing page lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s (this used smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s (this used largest known Diffusivity @ 30°C).

Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C, 35°C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified) Maximum Percent Relative Humidity

Maximum Percent Relative Humidity												
Package Type and Body Thickness	**Moisture Sensitivity Level**	**5%**	**10%**	**20%**	**30%**	**40%**	**50%**	**60%**	**70%**	**80%**	**90%**	
Body Thickness ≥3.1 mm	Level 2a	∞	∞	94	44	32	26	16	7	5	4	35°C
Including		∞	∞	124	60	41	33	28	10	7	6	30°C
PQFPs >84 pin,		∞	∞	167	78	53	42	36	14	10	8	25°C
PLCCs (square)		∞	∞	231	103	69	57	47	19	13	10	20°C
All MQFPs	Level 3	∞	∞	8	7	6	6	6	4	3	3	35°C
or		∞	∞	10	9	8	7	7	5	4	4	30°C
All BGAs ≥1 mm		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	3	3	3	2	2	2	2	1	1	35°C
		∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	2	2	2	2	1	1	1	1	1	35°C
		∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	1	1	1	1	1	1	1	1	1	35°C
		∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm	Level 2a	∞	∞	∞	∞	58	30	22	3	2	1	35°C
≤ Thickness		∞	∞	∞	∞	86	39	28	4	3	2	30°C
<3.1 mm including		∞	∞	∞	∞	148	51	37	6	4	3	25°C
PLCCs (rectangular)		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
18-32 pin	Level 3	∞	∞	12	9	7	6	5	2	2	1	35°C
SOICs (wide body)		∞	∞	19	12	9	8	7	3	2	2	30°C
SOICs ≥20 pins,		∞	∞	25	15	12	10	9	5	3	3	25°C
PQFPs ≤80 pins		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	5	4	3	3	2	2	1	1	1	35°C
		∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	3	2	2	2	2	1	1	1	1	35°C
		∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	1	1	1	1	1	1	1	0.5	0.5	35°C
		∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm	Level 2a	∞	∞	∞	∞	∞	∞	17	1	0.5	0.5	35°C
including		∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
SOICs <18 pin		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
All TQFPs, TSOPs		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
or	Level 3	∞	∞	∞	∞	∞	8	5	1	0.5	0.5	35°C
All BGAs <1 mm body		∞	∞	∞	∞	∞	11	7	1	1	1	30°C
thickness		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	7	4	3	2	1	0.5	0.5	35°C
		∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	7	3	2	2	1	1	0.5	0.5	35°C
		∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	7	2	1	1	1	1	1	0.5	0.5	35°C
		∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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